

Pending Claims (this listing replaces all prior versions):

1. (currently amended) A method comprising:
~~from at least two types determining a type of endian conversion each of which can be performed on a portion of data stored within a memory system, determining a type; and writing an table entry to a memory management table based on the determining, that specifies the type of endian conversion to be performed on the portion of data.~~
2. (currently amended) The method of claim 1 wherein writing an table entry to a memory management table further includes specifying the location of the portion of data within the memory system.
3. (currently amended) The method of claim 1 wherein the ~~at least two types~~ type of endian conversion include [[is]] a data coherent conversion.
4. (currently amended) The method of claim 1 wherein the ~~at least two types~~ type of endian conversion include [[is]] an address coherent conversion.
5. (currently amended) The method of claim 1 wherein the table entry includes a single bit for specifying one of two types of endian conversion.
6. (currently amended) The method of claim 1 wherein the table entry maps a virtual memory address to a physical memory address.
7. (currently amended) A method comprising:
maintaining a memory management table that includes one or more table entries, each table entry defining a location of a portion of data stored within a memory system and indicating

a type determined from at least two types of endian conversion each of which can [[to]] be performed on the portion of data.

8. (currently amended) The method of claim 7 wherein the at least two types type of endian conversion include [[is]] a data coherent conversion.

9. (currently amended) The method of claim 7 wherein the at least two types type of endian conversion include [[is]] an address coherent conversion.

10. (currently amended) The method of claim 7 wherein the table entry includes a single bit for specifying one of the at least two types of endian conversion.

11. (original) The method of claim 7 wherein the portion of data is stored at a physical memory address within a memory system.

12. (currently amended) The method of claim 11 wherein the table entry maps the physical address at which the portion of data is stored to a virtual address accessible by a processor.

13. (currently amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

from at least two types determine a type of endian conversion each of which can be performed on a portion of data stored within a memory system, determine a type; and

write an table entry to a memory management table based on the determining, that specifies the location of the portion of data within the memory system and the type of endian conversion to be performed on the portion of data.

14. (currently amended) The computer program product of claim 13 wherein the at least two types type of endian conversion include [[is]] a data coherent conversion.

15. (currently amended) The computer program product of claim 13 wherein the at least two types type of endian conversion include [[is]] an address coherent conversion.

16. (currently amended) The computer program product of claim 13 wherein the table entry includes a single bit for specifying one of two types of endian conversion.

17. (currently amended) The computer program product of claim 13 wherein the table entry maps a virtual memory address to a physical memory address.

18. (currently amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

maintain a memory management table that includes one or more table entries each table entry defining a location of a portion of data stored within a memory system and indicating a type determined from at least two types of endian conversion each of which can [[to]] be performed on the portion of data.

19. (currently amended) The computer program product of claim 18 wherein the at least two types type of endian conversion include [[is]] a data coherent conversion.

20. (currently amended) The computer program product of claim 18 wherein the at least two types type of endian conversion include [[is]] an address coherent conversion.

21. (currently amended) The computer program product of claim 18 wherein the table entry includes a single bit for specifying one of the at least two types of endian conversion.

22. (original) The computer program product of claim 18 wherein the portion of data is stored at a physical memory address within a memory system.

23. (currently amended) The computer program product of claim 2219 wherein the table entry maps the physical address at which the portion of data is stored to a virtual address accessible by a processor.

24. (currently amended) A memory management table residing in computer memory comprising:

one or more table entries, with each table entry having a first field for defining the location of a portion of data stored within a memory system and a second field for defining a type determined from at least two types of endian conversion each of which can [[to]] be performed on the portion of data.

25. (currently amended) The memory management table of claim 24 wherein each table entry includes a single bit for specifying one of the at least two types of endian conversion.

26. (currently amended) The memory management table of claim 24 [[25]] wherein one type the at least two types of endian conversion include [[is]] a data coherent conversion.

27. (currently amended) The memory management table of claim 24 [[25]] wherein one type the at least two types of endian conversion include [[is]] an address coherent conversion.

28. (currently amended) The memory management table of claim 24 [[25]] wherein each table entry maps a virtual memory address to a physical memory address.

29. (currently amended) A system comprising:

a first processor for processing data in a first endian format;

a second processor for processing data in a second endian format;

a bus for interconnecting the first and second processors;

an endian converter for converting portions of data from the first endian format to the second endian format; and

a memory management table including one or more ~~table~~ entries, with each ~~table~~ entry defining a location for a portion of data to be converted from the first endian format to the second endian format, and indicating a type determined from at least two types of endian conversion each of which can [[to]] be performed on the portion of data by the endian converter.

30. (currently amended) The system of claim 29 wherein the at least two types type of endian conversion include [[is]] a data coherent conversion.

31. (currently amended) The system of claim 29 wherein the at least two types type of endian conversion include [[is]] an address coherent conversion.

32. (original) The system of claim 29 wherein the first processor is a little-endian processor.

33. (original) The system of claim 29 wherein the second processor is a big-endian processor.

34. (currently amended) A computer architecture comprising:
a networking device, including:
a first processor for processing data in a first endian format;
a second processor for processing data in a second endian format;
a bus for interconnecting the first and second processors;
an endian converter for converting portions of data from the first endian format to the second endian format; and

a memory management table including one or more ~~table~~ entries, with each ~~table~~ entry defining a location for a portion of data to be converted from the first endian format to the second endian format, and indicating a type determined from at least two types of endian conversion each of which can [[to]] be performed on the portion of data by the endian converter.

35. (currently amended) The architecture of claim 34 wherein the at least two types type of endian conversion include [[is]] a data coherent conversion.

36. (currently amended) The architecture of claim 34 wherein the at least two types type of endian conversion include [[is]] an address coherent conversion.

37. (original) The architecture of claim 34 wherein the first processor is a little-endian processor.

38. (original) The architecture of claim 34 wherein the second processor is a big-endian processor.

39. (currently amended) A method comprising:
accessing a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator; and

from at least two types determining a type of endian conversion each of which can be performed on the portion of data, determining a type based on the conversion-type indicator.

40. (currently amended) The method of claim 39 wherein the at least two types type of endian conversion include is a data coherent conversion.

41. (currently amended) The method of claim 39 wherein the at least two types type of endian conversion include is an address coherent conversion.

42. (original) The method of claim 39 wherein the conversion-type indicator includes a single bit for specifying one of the at least two types of endian conversion.

43. (currently amended) A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

access a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator; and

from at least two types determine a type of endian conversion each of which can be performed on the portion of data, determine a type based on the conversion-type indicator.

44. (currently amended) The computer program product of claim 43 wherein the at least two types type of endian conversion include is a data coherent conversion.

45. (currently amended) The computer program product of claim 43 wherein the at least two types type of endian conversion include is an address coherent conversion.

46. (currently amended) The computer program product of claim 43 wherein the conversion-type indicator includes a single bit for specifying one of the at least two types of endian conversion.

47. (currently amended) A method comprising:

from at least two types determining a type of endian conversion each of which can be performed on a portion of a page stored within a memory system, determining a type; and writing an table entry to a memory management table based on the determining. that specifies the type of endian conversion to be performed on the portion of the page.

48. (currently amended) The method of claim 47 wherein writing an table entry to a memory management table further includes specifying the location of the portion of the page within the memory system.

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49. (currently amended) The method of claim 47 wherein the at least two types type of endian conversion include is a data coherent conversion.

50. (currently amended) The method of claim 47 wherein the at least two types type of endian conversion include is an address coherent conversion.